

Potential Future Generation Nanoscale MOS Device: *Trigate (TG)* or *Double Gate (DG)* *FinFETs*?

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Abstract—Performance limit of Tri-Gate (TG) and Double Gate (DG) SOI FinFETs have been compared in terms of ballistic current which is calculated using a modified model shown for conventional MOSFET. Such a simple model for calculating ballistic current in nanoscale multigate MOSFETs is yet to be reported. Comparison of the ballistic current for different Si fin thicknesses reveals that for decreasing fin thickness, strong quantum mechanical confinement degrades the ballistic current. The simulation result presented here contradicts with the previously reported result that TG FinFETs show better performance than DG FinFET and reveals that DG FinFET shows slightly better performance below $5nm$ fin thickness. This result indicates that in terms of ballistic drive current the tri-gate device is not always favorable than double gate device especially when the device dimension is scaled down deeply.

I. INTRODUCTION

Multi-gate FETs, especially FinFETs, appear to be superior alternatives to replace the conventional bulk MOSFETs to continue scaling down to a $10nm$ feature size [1]. In such nanoscale regime, where device dimension becomes comparable to the mean free path of carrier, ballistic transport is prominent. Volume inversion in sub $10nm$ fin thickness reduces the scattering effect considerably [2] and Monte Carlo simulation shows that drive current in sub $15nm$ long channel transistor is very close to the value obtained in the ballistic limit in spite of the presence of some scattering effects [2], [3]. NEGF based quasi 3D numerical model [4] and 3D NEGF quantum transport simulator based on CBR [5] have been reported to study ballistic transport in multigate devices. However, a simple ballistic current model using 2D simulation for nanoscale FinFETs is yet to be reported. In this paper, a self consistent solver is used to calculate the ballistic current in *Tri-Gate (TG)* and *Double Gate (DG) SOI FinFETs* by modifying the model shown in [6]. The model shown in [6] for 1D MOSFET is modified to be applicable for self consistent solution of coupled 2D Poisson-Schrödinger equation. The self consistent simulation is done along the plane perpendicular to the transport direction (Fig. 1) [7]. However, In [7], classical

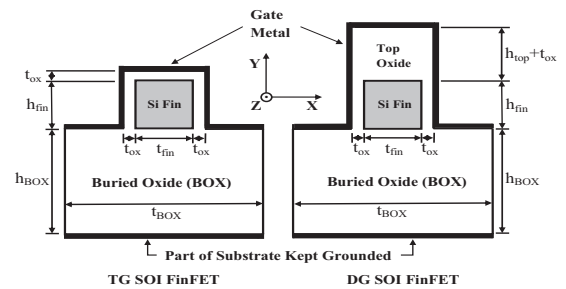


Fig. 1. Device Structures

drift-diffusion model is used for long channel device. In this paper, the charge calculation is done self consistently and ballistic current is calculated for small channel length using the modified approach shown in [6]. Finally, a comparative benchmarking is done on the basis of ballistic current limit for the variation in silicon fin thickness. In [5], current in TG FinFET is found to be greater than DG FinFET. However, the comparative study presented here contradicts with reported result for deep scaling in silicon fin thickness and reveals that below $5nm$ fin thickness TG FinFETs give less drive current than that of DG FinFETs. However, consistency is found in the simulated results with the experimental results indicating the validity of the proposed modification in the model shown in [6].

II. RESULTS AND DISCUSSIONS

Silicon fin thickness or fin width, which is one of the most important process parameters of FinFET, has been varied to observe the changes in ballistic current. As shown in Fig. 2, the energy of the populated subbands increases with decreased fin width along with an increase in the difference between *1st* and *2nd* subband energies because of increased quantum confinement which is consistent with the result reported in [8]. The increased quantization effect is due to the deeper quantum well with decreasing dimension, which is consistent with the results obtained for long channel devices in [7]. The presence of thick oxide layer under the top gate of DG FinFET causes less amount of inversion charge whereas the amount is significantly higher when the same voltage is applied to a TG FinFET (Fig. 3). However as the fin width decreases,

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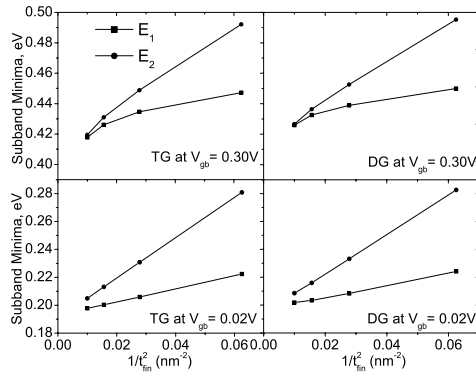


Fig. 2. Minimum subband energy of 1st and 2nd subband at different gate voltages for TG and DG SOI FinFETs as a function of $\frac{1}{t_{fin}^2}$, where t_{fin} denotes silicon fin thickness

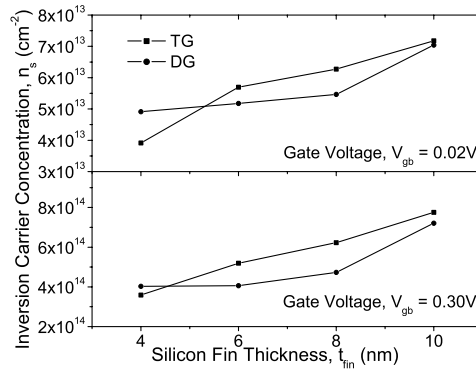


Fig. 3. Inversion carrier concentration as a function of silicon fin thickness for TG and DG SOI FinFETs at two gate voltages for a drain voltage $V_{ds} = 0.5V$

the difference is less visible because of increased quantum confinement where the presence or absence of an additional gate on the top edge of silicon fin has little or no effect on the total charge concentration. So as shown in Fig. 3, the inversion carrier concentration is comparable for TG and DG FinFETs when device dimension is scaled below $5nm$ with a slight increase for DG FinFET when the fin thickness is $4nm$. The on-current in this model is directly proportional to the carrier concentration [6]. Fig. 4 shows that drain current trend shows almost same dependency on fin thickness, becoming greater in DG FinFET than TG FinFET at a fin thickness of $4nm$. Although the effect of an increase in the gate on top in TG FinFET is reported to result in higher drive current [5], the result shown here contradicts with the previous result. From this result it can be concluded clearly that an increase in the number of gate does not necessarily increase current which also depends on the device dimension and the drive current dependency on the top gate becomes weak as fin thickness is scaled down. For a constant gate voltage, both TG and DG exhibit the common I-V characteristics (Fig. 5) consistent with the results shown previously in both experimental and simulation based works [1], [5].

A simple ballistic current model for multigate FinFETs is proposed and the impact of fin width variation on subband

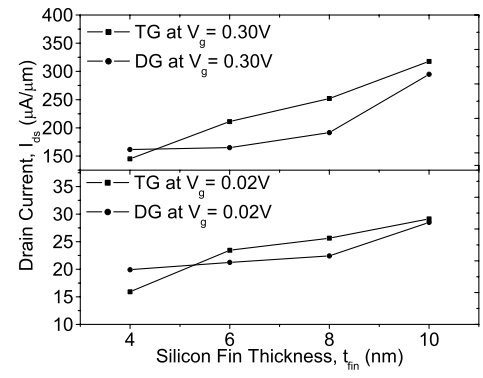


Fig. 4. Drain current as a function of silicon fin thickness for TG and DG SOI FinFETs at two different gate voltages for a drain voltage $V_{ds} = 0.5V$

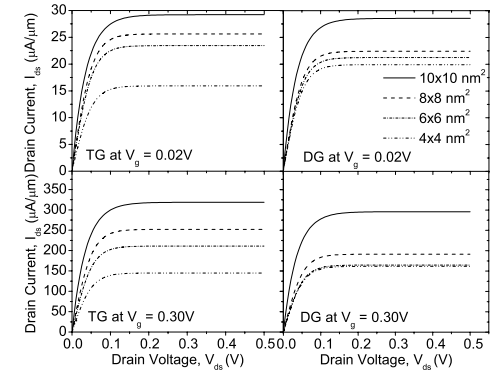


Fig. 5. Drain current as a function of drain voltage for TG and DG SOI FinFETs at two different gate voltages with a variation in silicon fin thickness

energies, inversion charge density and drain current has been studied. The result shows that the strong quantum confinement plays a prominent role when fin dimensions are scaled down beyond $10nm$ regime and causes the drive current of TG and DG FinFETs to come closer. This phenomenon suggest that ballistic transport in multigate FinFETs becomes less dependent on the number of gates if fin width is decreased.

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